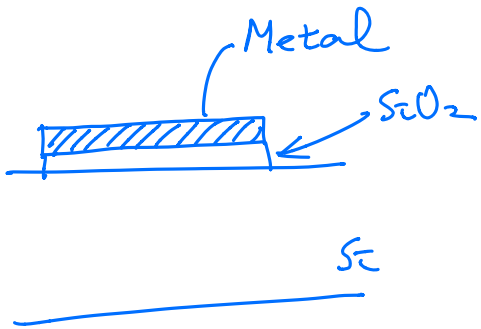

EE105
Microelectronic Devices and Circuits:
MOS Capacitor

Metal oxide semiconductor

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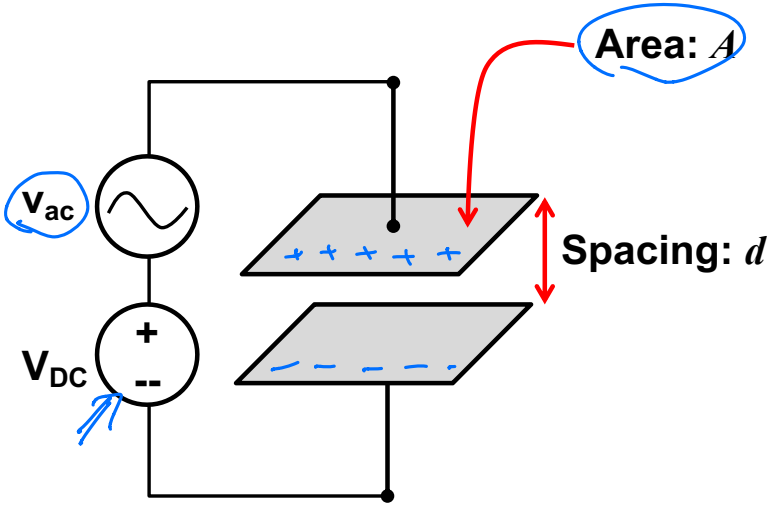
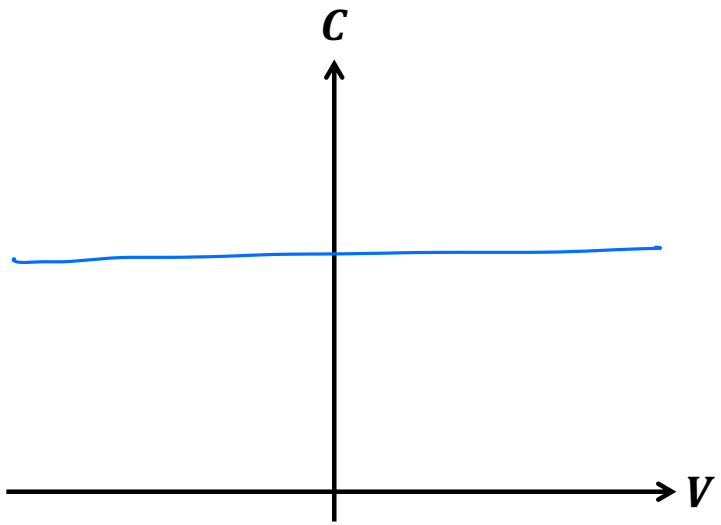
Linear Capacitor

$$C = \frac{\epsilon A}{d}$$

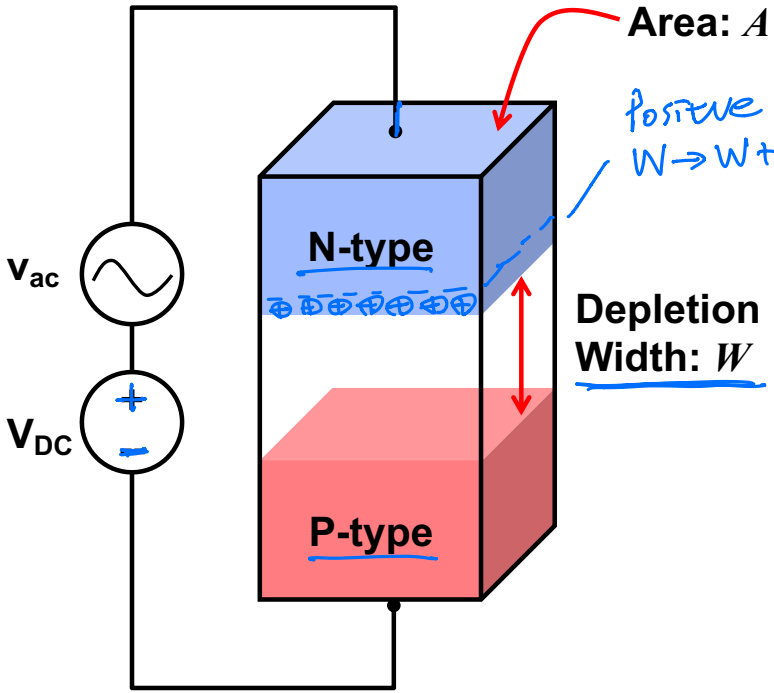
Area

spacing





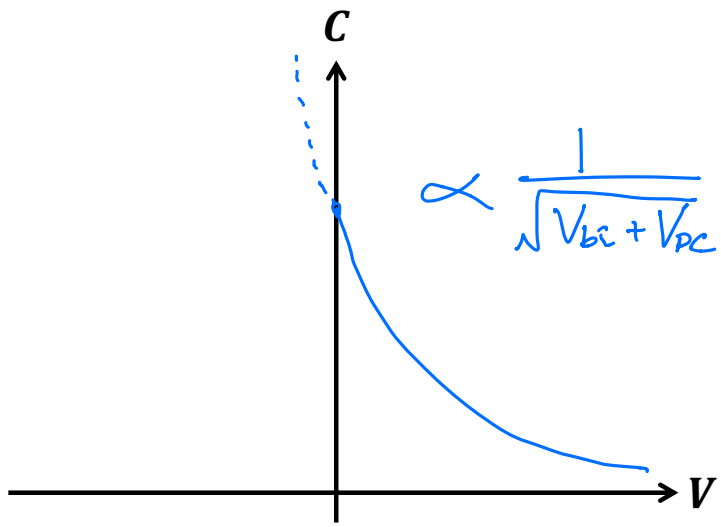
Nonlinear Capacitor – Reverse-Biased PN Junction



positive cycle
$W \rightarrow W + \Delta W$

$$C = \frac{\epsilon A}{W}$$

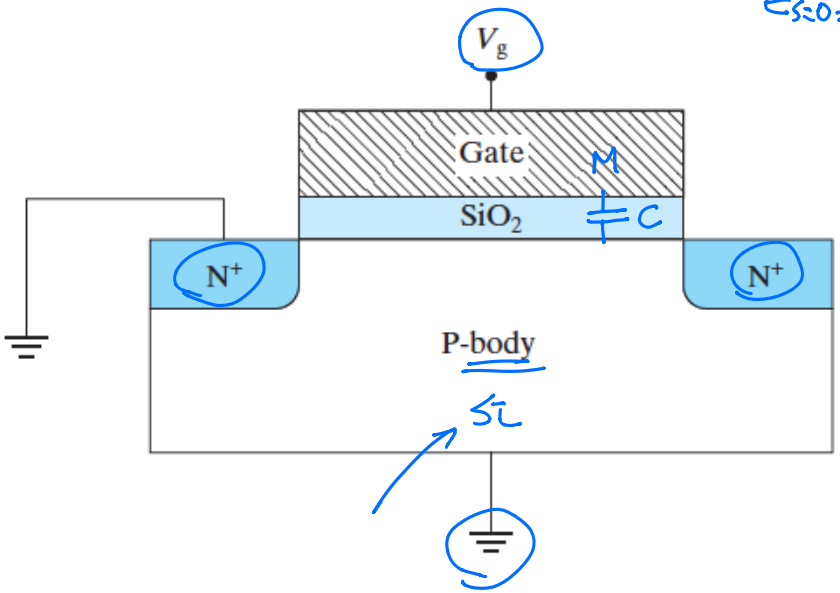
$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)(V_{bi} + V_{DC})}$$



Behave exactly like parallel plate cap

Metal-Oxide-Semiconductor (MOS): Integral Part of MOS Transistor

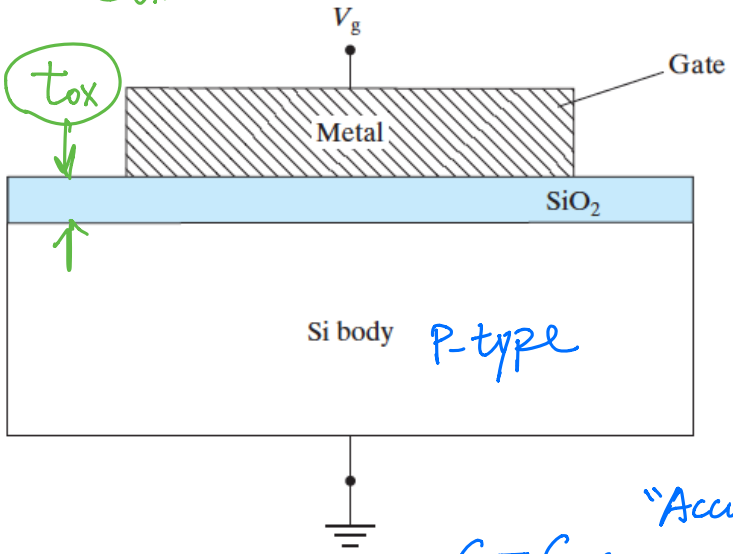
$\epsilon_{SiO_2} = 3.9 \cdot \epsilon_0$



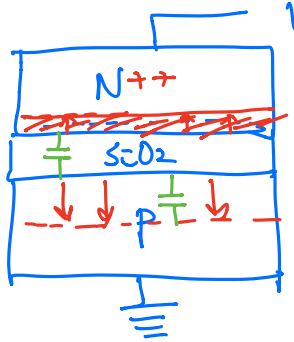
Metal-Oxide-Semiconductor (MOS) Capacitor

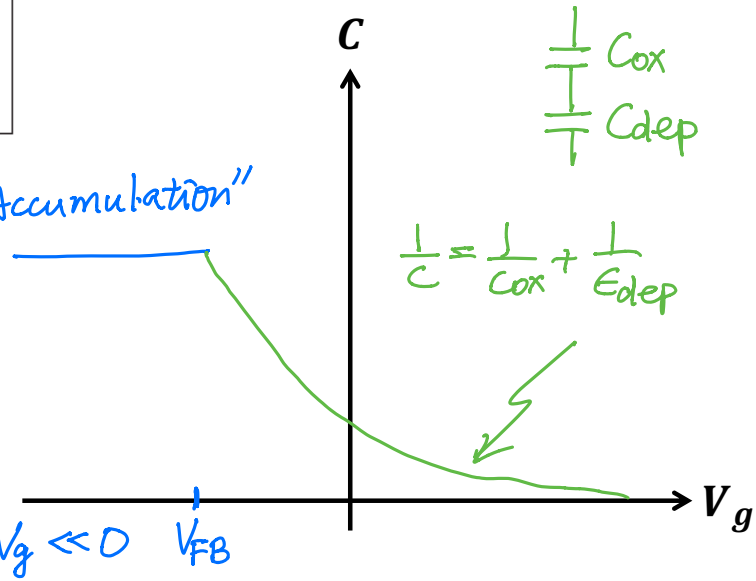
$\epsilon_{Si} \sim 12 \cdot \epsilon_0$

$\epsilon_{ox} \sim 4\,\epsilon_0$



Think





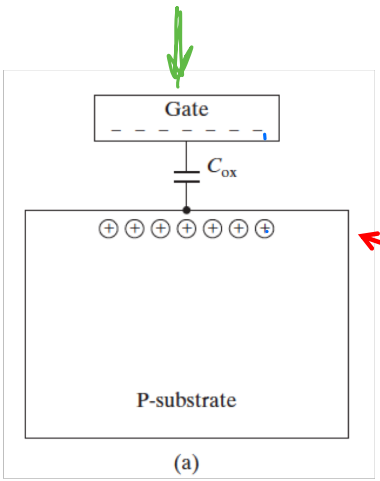
V_{FB} = Flat Band

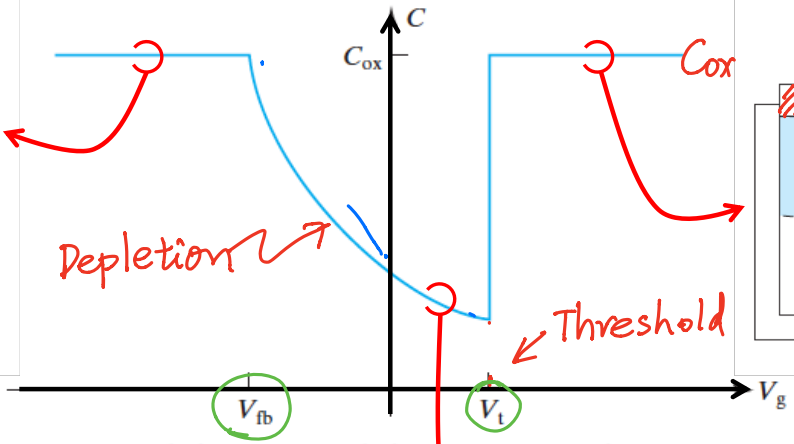
C_{dep} = depletion cap. = $\frac{\epsilon_{Si}}{W}$

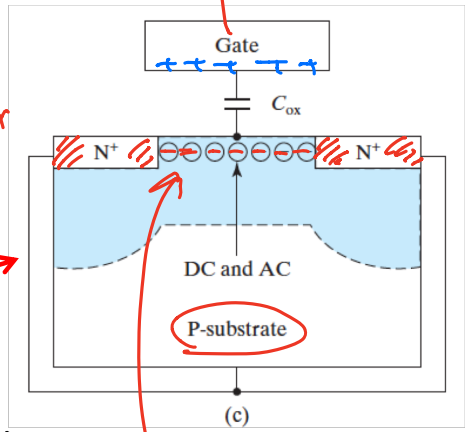
C_{ox} = oxide cap = $\frac{\epsilon_{SiO_2}}{t_{ox}} = \frac{\epsilon_{ox}}{t_{ox}}$

t_{ox} : thickness of oxide

C-V Curve of MOS Capacitor







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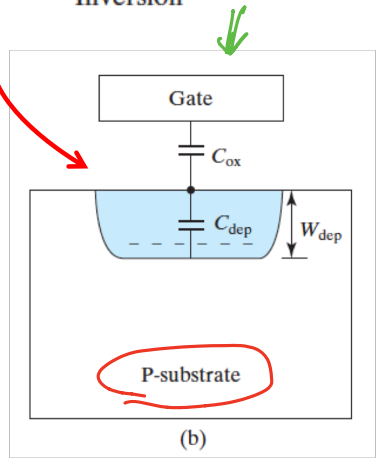
Flat-band voltage : V_{fb}

Threshold voltage:

$$V_t = V_{fb} + 2\frac{kT}{q} ln\left(\frac{N_a}{n_i}\right) + \frac{\sqrt{qN_a 2\epsilon_s 2\phi_B}}{C_{ox}}$$



Sheet of electrons induced by gate voltage

⇒ Parallel cap.

$C = C_{ox}$

⇒ Channel